

SUBSTRATE FOR MOUNTING A SEMICONDUCTOR CHIP AND METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

5 BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a substrate for mounting of a semiconductor chip, and to a method for manufacturing a semiconductor device .

Description of the Related Art

10 A substrate for mounting of a semiconductor chip (mounting substrate) generally has a plurality of mounting regions as shown in Fig. 6(A). A semiconductor device is conventionally mounted as described below.

Semiconductor chips 52 are mounted on mounting regions 60a-60d of a mounting substrate 50, respectively. Pads 54 of each semiconductor chip are
15 connected by bonding wires to inner electrodes 56 of a corresponding mounting region. The mounting regions 60a-60d are then filled with resin, and the mounting substrate 50 is diced into individual semiconductor devices.

As seen in Fig. 6(B), inner electrodes 56a and 56b are formed on the mounting substrate 50, and each inner electrode 56a, 56b is connected to outer
20 electrode via through holes (not shown). These inner electrodes 56 are generally formed by electroplating. All of the inner electrodes 56 are electrically and physically connected to each other by an interconnection 58 before the mounting substrate 50 is diced into individual semiconductor devices. However,

after dicing, the inner electrodes 56 should be electrically isolated from one another.

The interconnect wiring pattern 58 corresponds to the dicing line, and the interconnect wiring pattern 58 is supposed to be removed by a dicing blade during dicing the mounting substrate. However, if the position of the dicing blade is shifted, a portion of the interconnect wiring pattern 58 remains as shown in Fig. 6(C). In some cases, the remaining portion of the interconnect wiring pattern 58 connects one inner electrode to another inner electrode, thus short-circuiting the inner electrodes.

SUMMARY OF THE INVENTION

An object of the present invention is to solve the above-described problem.

According to one aspect of this invention, for achieving the above object, A mounting substrate includes a substrate body having at least first and second adjacent chip mounting regions defined on a surface thereof, and further having a dicing line defined between the first and second mounting regions; a first plurality of inner electrodes aligned along a first side of the first chip mounting region, a second plurality of inner electrodes aligned along a second side of the second chip mounting region, wherein the first side of the first chip mounting region confronts the second side of the second chip mounting region, an interconnect wiring pattern located between the first and second chip mounting

region, and commonly connected to the first plurality of inner electrodes and the second plurality of inner electrodes, wherein the interconnect wiring pattern includes a plurality of connected wiring portions , and wherein at least some of said wiring pattern extend obliquely across the dicing line.

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BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and
10 further objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings, in which:

Fig. 1(A) is a top view diagram showing a substrate for mounting a semiconductor chip according to a first embodiment of the present invention;

15 Fig.1(B) is an enlarged view of a boundary portion between mounting regions;

Fig. 2(A)-(D) are process diagrams illustrating process steps employed in a method using a mounting substrate of the present invention.;

20 Fig.3(A)-(B) are enlarged diagrams showing a boundary portion between mounting regions after dicing;

Fig.4 (A)-(B) are enlarged diagrams showing a boundary portion between mounting regions according to another example of the present invention;

Fig.5 (A)-(B) are enlarged diagrams showing a boundary portion between

mounting regions according to another example of the present invention; and

Fig.6(A)-(C) are schematic diagrams of the prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

5 Preferred embodiments of the present invention will hereinafter be described in detail with reference to the accompanying drawings.

A mounting substrate 10 of this embodiment has a plurality of mounting blocks as shown in Fig. 1(A), with each mounting block having four mounting regions 20a-20d. Each mounting region has a plurality of inner electrodes 16 on
10 its peripheral portion, and a die pad 24 on its central portion where a semiconductor chip 12 is fixed thereon.

A semiconductor chip 12 is mounted on each mounting region. Pads 14 of each semiconductor chip are connected to inner electrodes 16 of a corresponding mounting region by wires. Each inner electrode 16 is connected to outer
15 electrodes via through holes. Pads 14 on one semiconductor chip are electrically connected to outer electrodes via through holes and inner electrodes 16.

Interconnect wiring pattern 26 are formed on the boundary portion between mounting regions in this embodiment. (For example, between regions 20a and 20b, regions 20b and 20c, regions 20c and 20d, and regions 20d and
20 20a). The interconnect wiring pattern 26 connect inner electrodes 16 of one mounting region to the inner electrodes of another mounting region prior to dicing. As shown in Fig. 1(B), the interconnect wiring pattern configured in a zig-zag pattern according to the present embodiment.

In particular, the mounting substrate 10 has first plurality of inner electrodes 16a arranged in line near the edge of first mounting region 20a. It also has second plurality of inner electrodes 16b arranged in line near the edge of second mounting region 20b. The edge of the second mounting region 20b is adjacent to the edge of the first mounting region 20a.

A dicing line 22 is defined between the first plurality of inner electrodes and the second plurality of inner electrodes. The interconnect wiring pattern 26 is located between the first and second chip mounting region, and commonly connected to the first plurality of inner electrodes and the second plurality of inner electrodes. The interconnect wiring pattern 26 of this embodiment do not have a portion which extends coincident with the dicing line 22. Each interconnect wiring pattern 26 is formed by electroplating to electrically connect the inner electrodes 16 using electroplating. However, they should not have an extending portion in the same direction of dicing line 22, especially near the boundary between the mounting regions 20.

The interconnect wiring pattern 26 of this embodiment includes a plurality of connected wiring portions in which at least some of the wiring pattern extend obliquely across the dicing line 22.

Fig.2 shows a schematic diagram for describing a method for manufacturing a semiconductor device using this mounting substrate.

Semiconductor chips 12 are fixed on mounting regions 20a-20d of a mounting substrate 10, respectively. Pads 14 of each semiconductor chip are connected to the inner electrodes 16 of a corresponding mounting region using

bonding wire. (Fig.2(A))

Then, each mounting block is filled with resin 30 as shown in Fig.2(B). A dicing tape 32 is adhered on the surface of the molded resin 30. The mounting substrate 10 is diced into individual semiconductor devices 40. (Fig.2(C)) Solder bumps 17 are then formed on outer electrodes of the mounting substrate. (Fig. 2.(D))

Fig. 3(A) and Fig. 3(B) shows a schematic diagram of the mounting substrate after dicing.

As shown in Fig. 3(A) and 3(B), each inner electrode 16 is electrically isolated because the interconnect wiring pattern 26 do not have an extending portion corresponding to the dicing line 22. A narrow dicing blade can be used because the interconnect wiring pattern 26 are formed in a zigzag pattern. Therefore, the width of a boundary portion can be decreased. The number of semiconductor devices formed in one mounting substrate thus can be increased.

Fig.4(A), which contains the same reference numbers to denote like elements as Fig. 1, shows another example of achieving the effects of this invention. Fig. 4(B) shows a schematic diagram of the mounting substrate of Fig. 4(A) after dicing. The interconnect wiring pattern 26 of this embodiment includes a plurality of connected wiring portions in which at least some of the wiring pattern extend obliquely across the dicing line 22. Other wiring patterns of the interconnect wiring pattern extend at right angle across the dicing line 22. This pattern does not have an interconnect portion which extends in the same direction as the dicing line 22..As can be seen from Fig.4(B), the inner electrodes

16 are electrically isolated one another after dicing.

Fig.5(A), which contains the same reference numbers to denote like elements as Fig. 1, shows another example of achieving the effects of this invention. Fig. 5(B) shows a schematic diagram of the mounting substrate of Fig. 5(A) after dicing. The interconnect wiring pattern 26 of this embodiment includes a plurality of connected wiring portions in which at least some of the wiring pattern extend obliquely in one direction across the dicing line 22. Other wiring patterns of the interconnect wiring pattern extend obliquely in another direction across the dicing line 22. This pattern does not have an interconnect portion which extends in the same direction as the dicing line 22..As can be seen from Fig.5(B), the inner electrodes 16 are electrically isolated one another after dicing.

According to this invention, short-circuiting of the inner electrodes after dicing is avoided The manufacturing efficiency is thus improved.